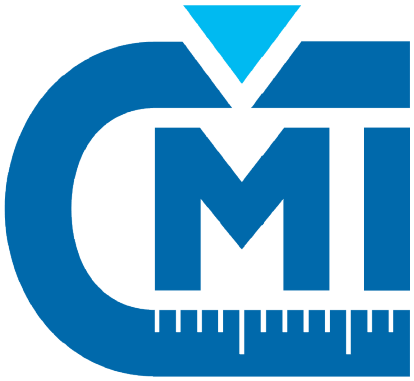
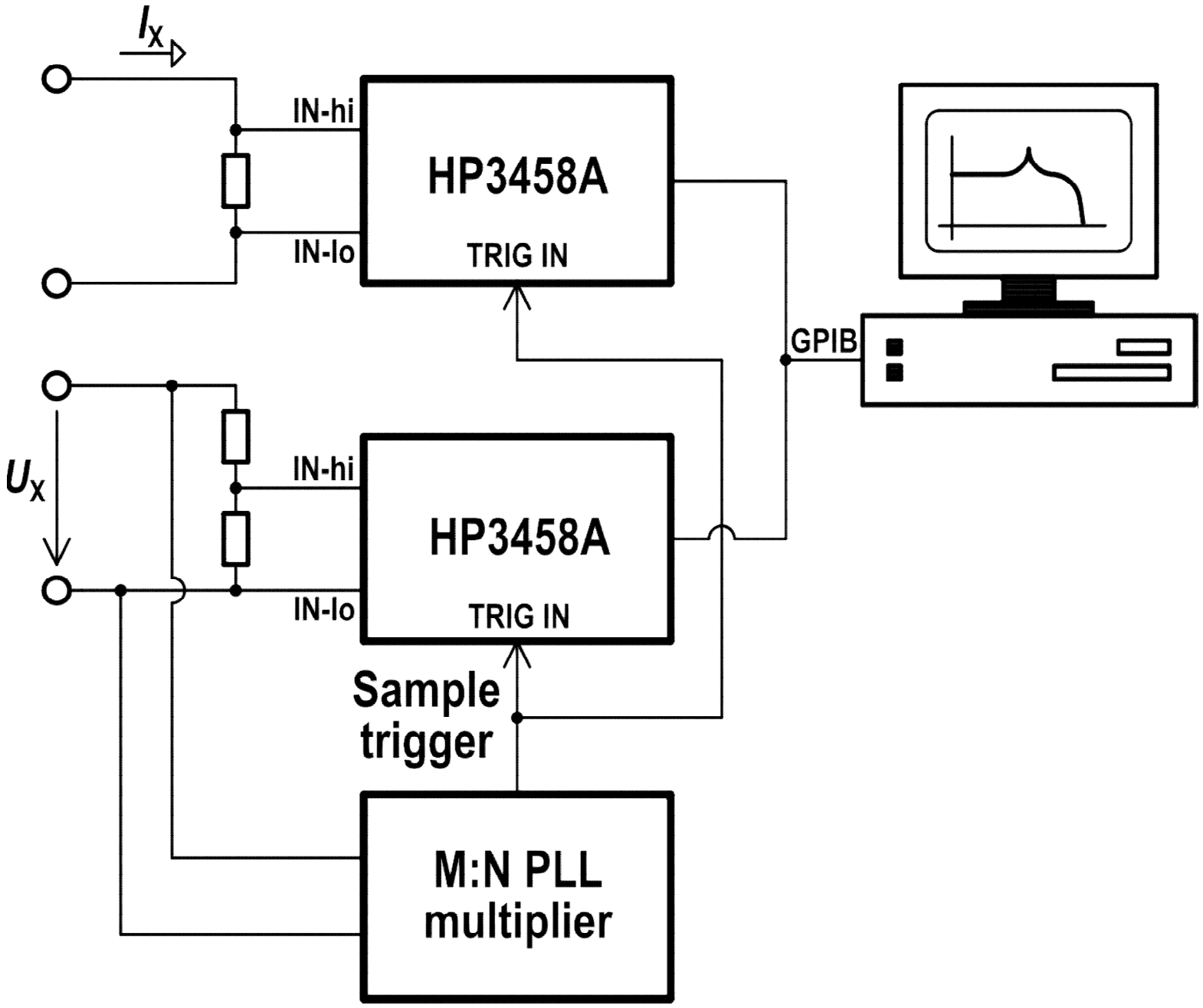


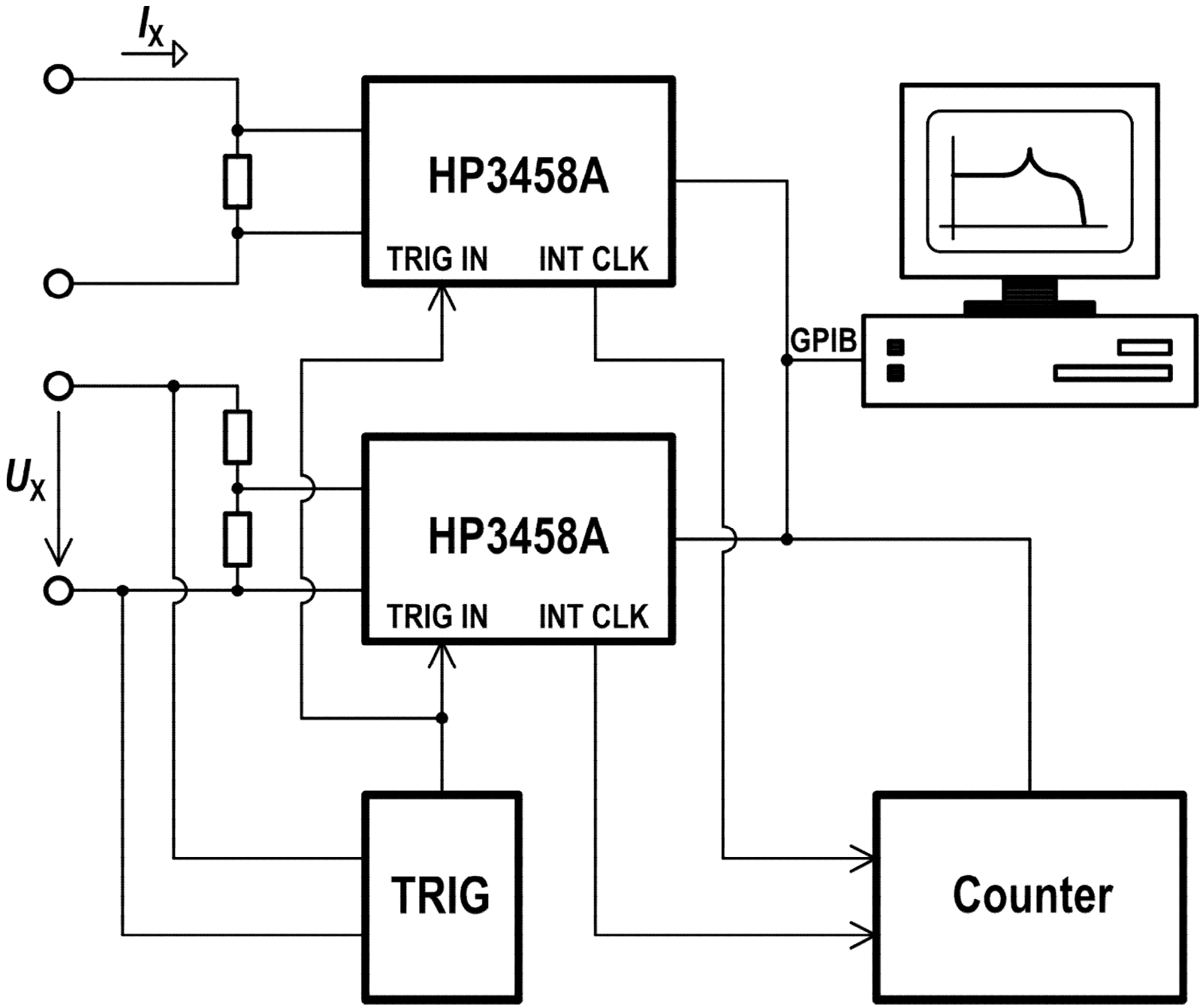
Czech Metrology Institute

Synchronization of HP3458A

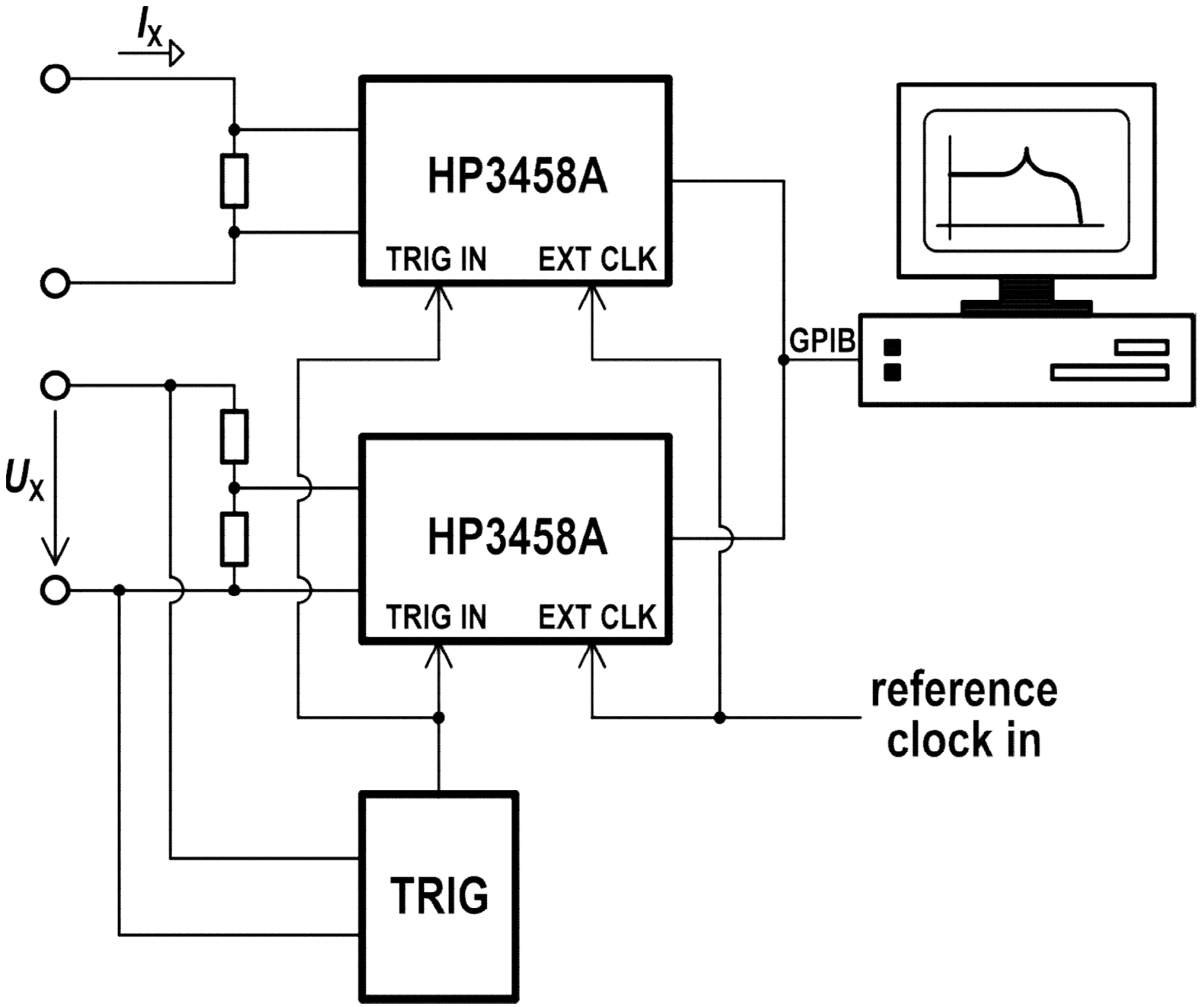
Basic synchronization 3458A



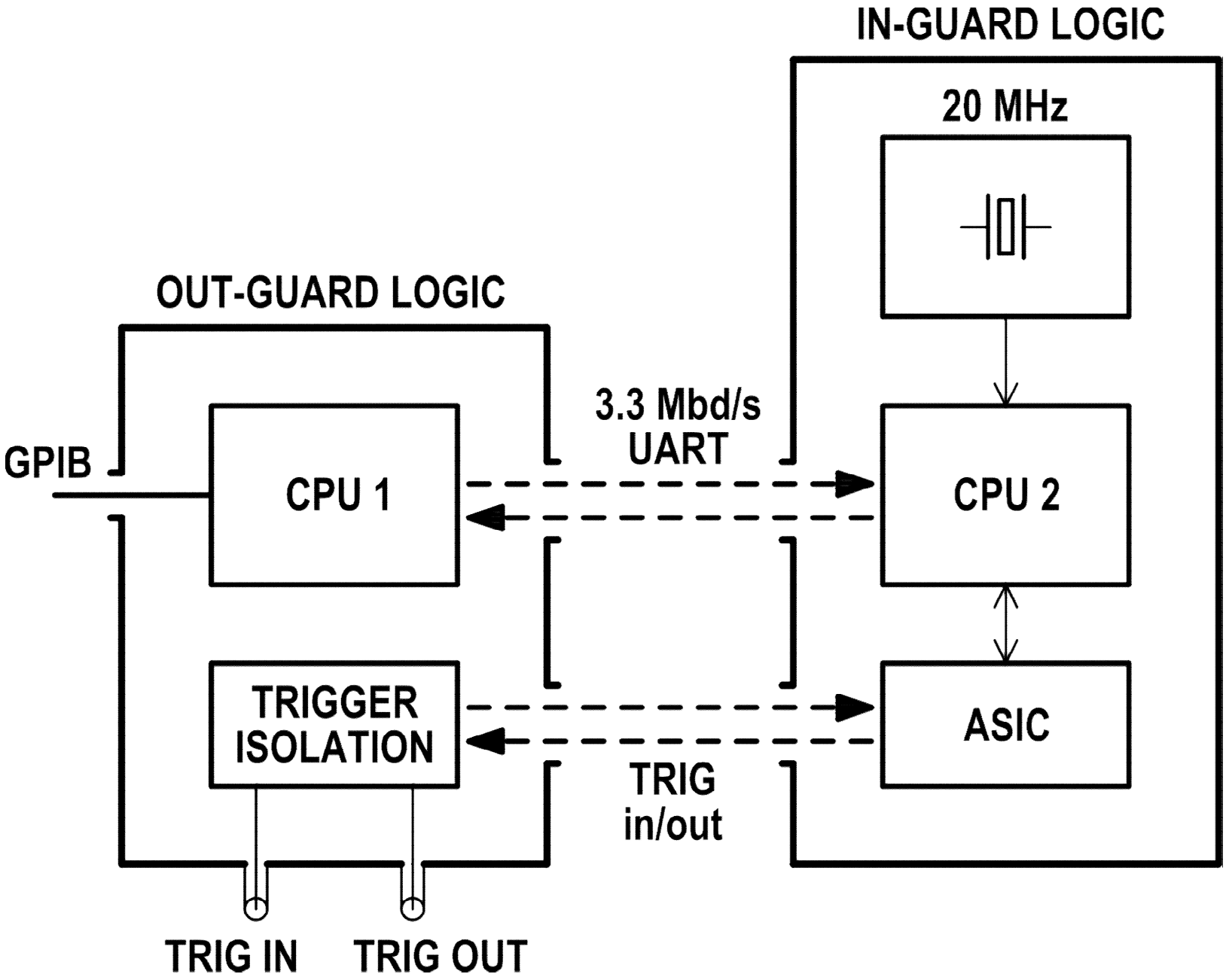
Basic synchronization 3458A



Basic synchronization 3458A



3458A insides



PLL version v1

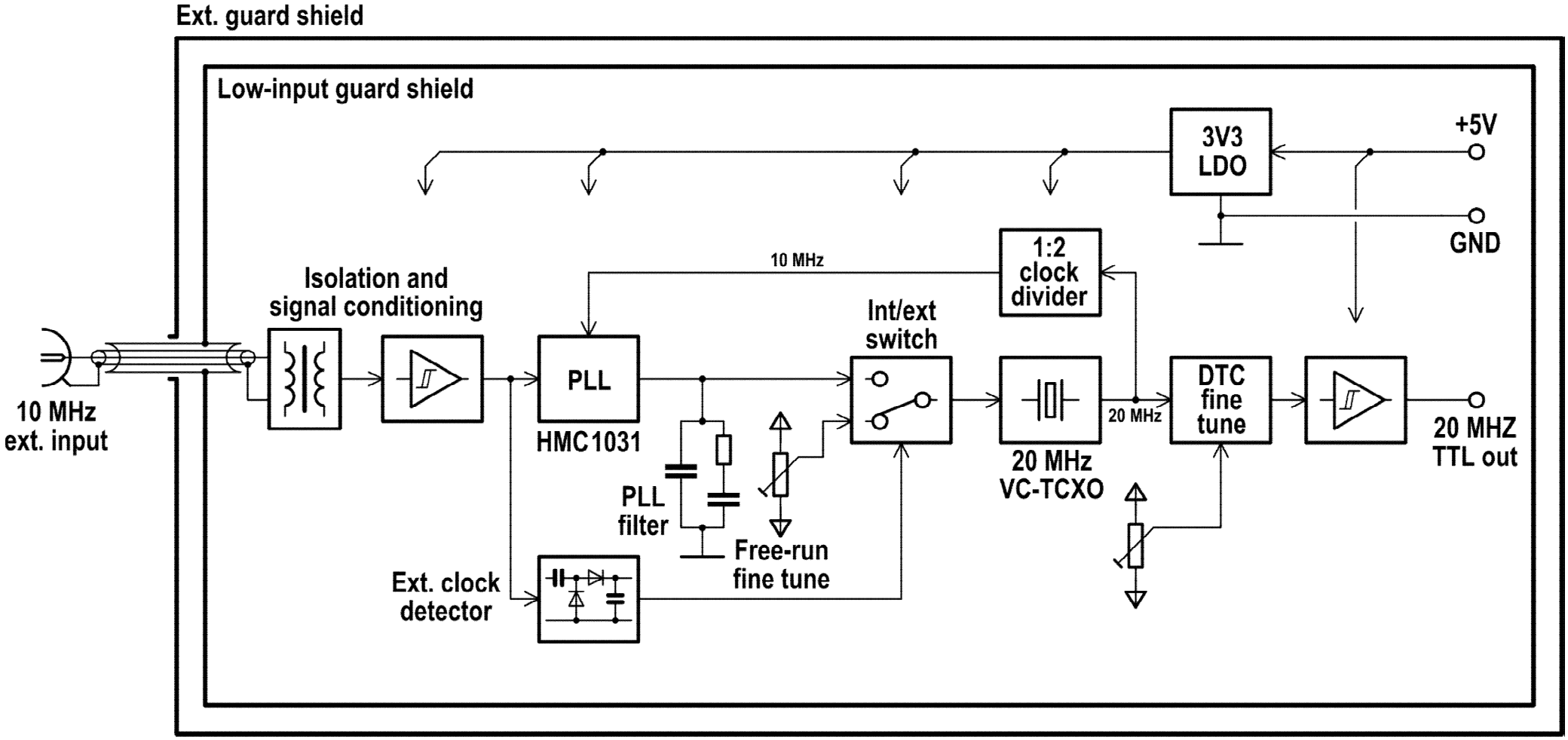
- So called “low jitter” PLL chip NB3N502 (15 ps rms)
- External clock autodetection
- Clock range ±1%
- Full isolation from external clock

- Result:
  - To high jitter, almost unstable

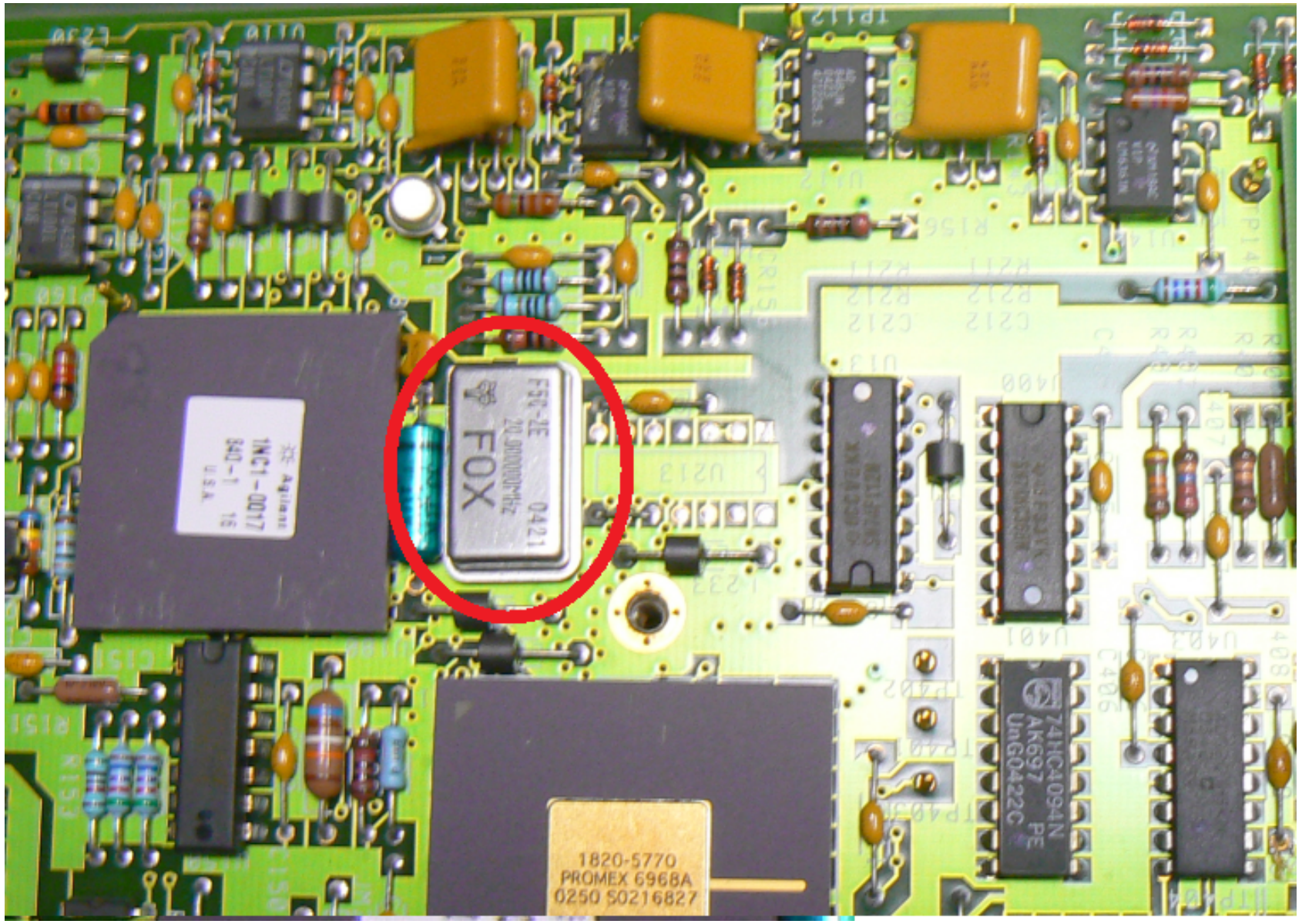
PLL version v2

- Based on PLL HMC1031 + VCTCXO
- Bandwidth < 10 Hz
- Clock range ±2 ppm
- Jitter approx. 1.5 ps rms
- External clock autodetection
- Free running clock error < 0.1 ppm
- Full isolation from external clock

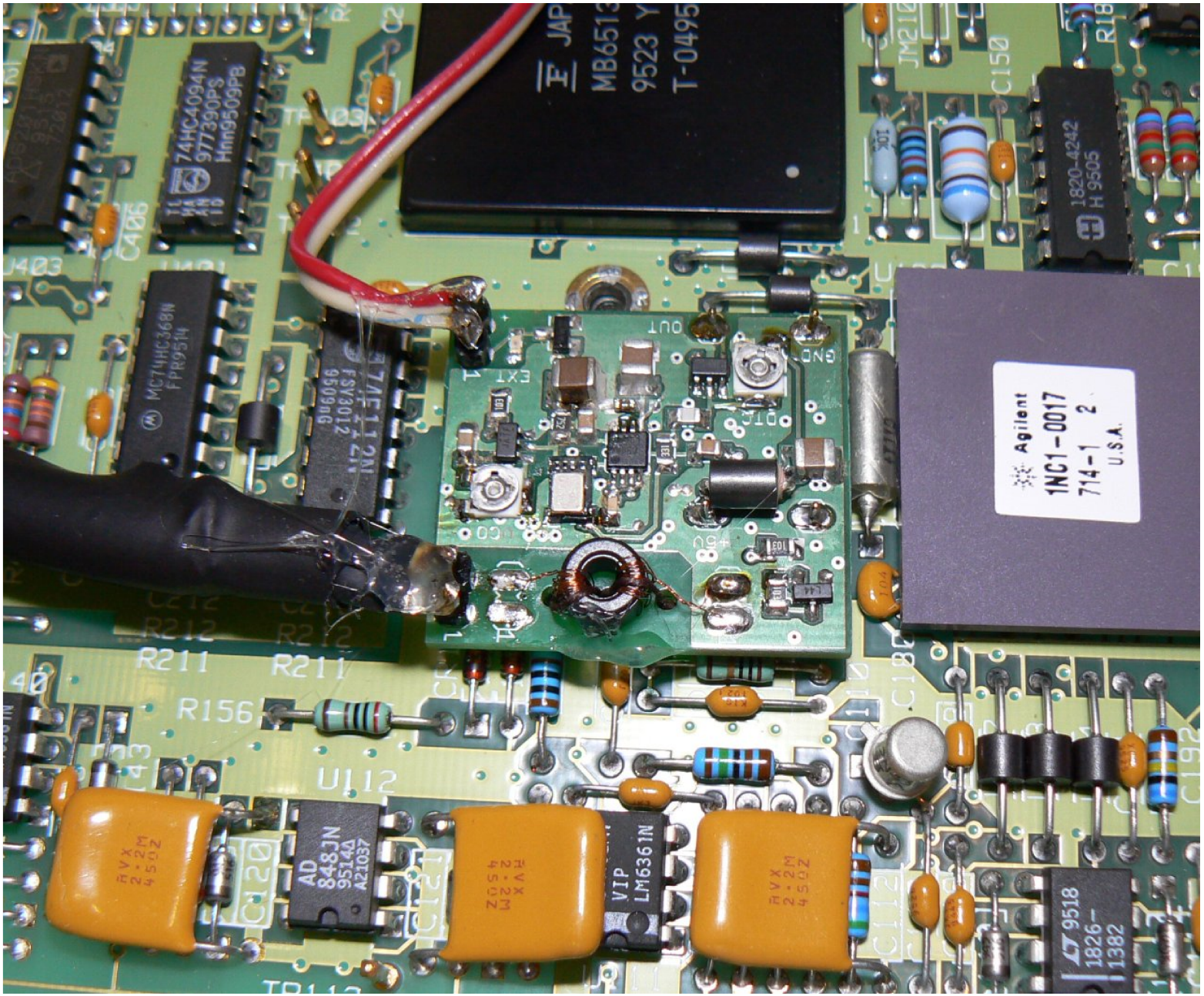
PLL version v2



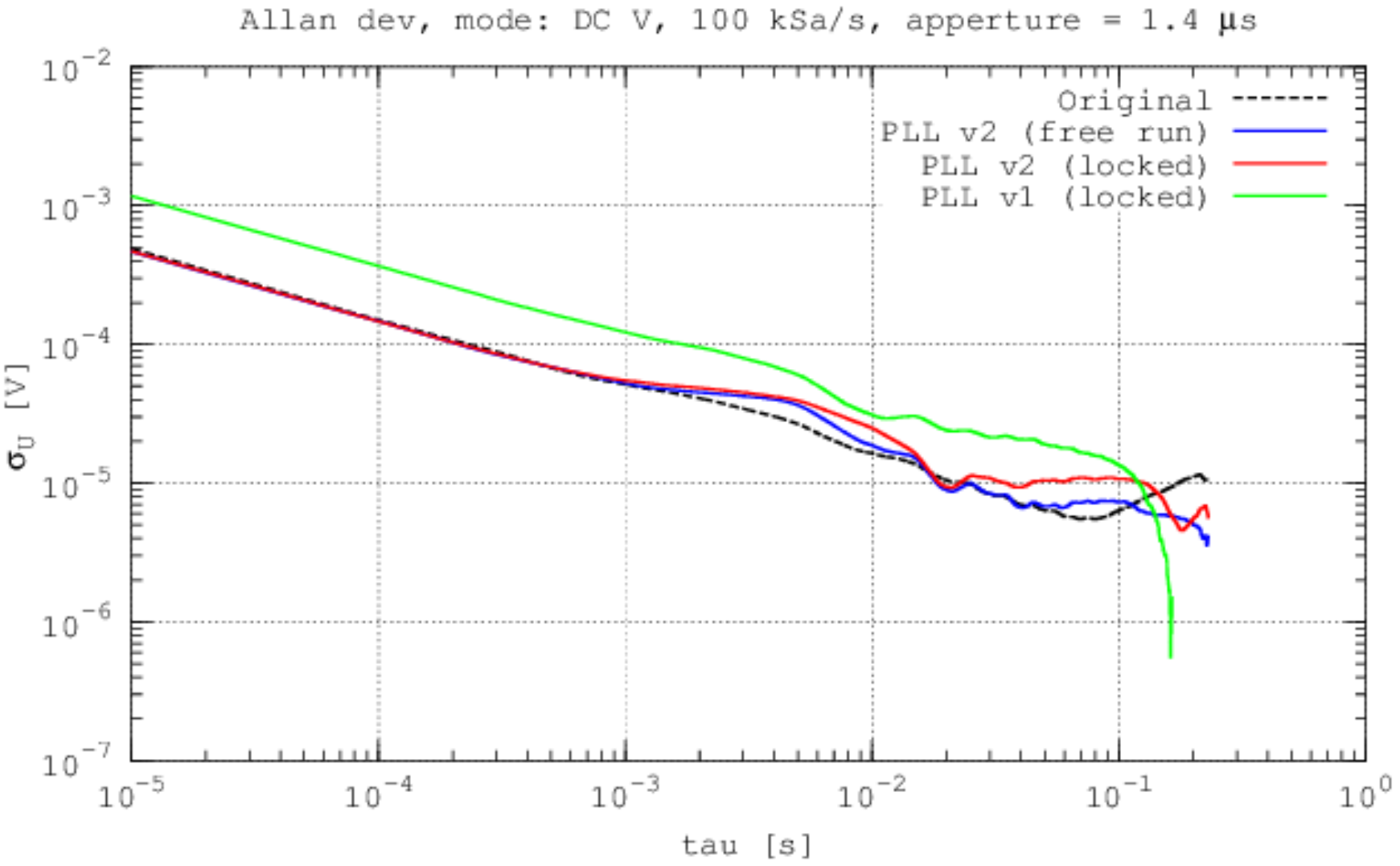
PLL version v2



PLL version v2

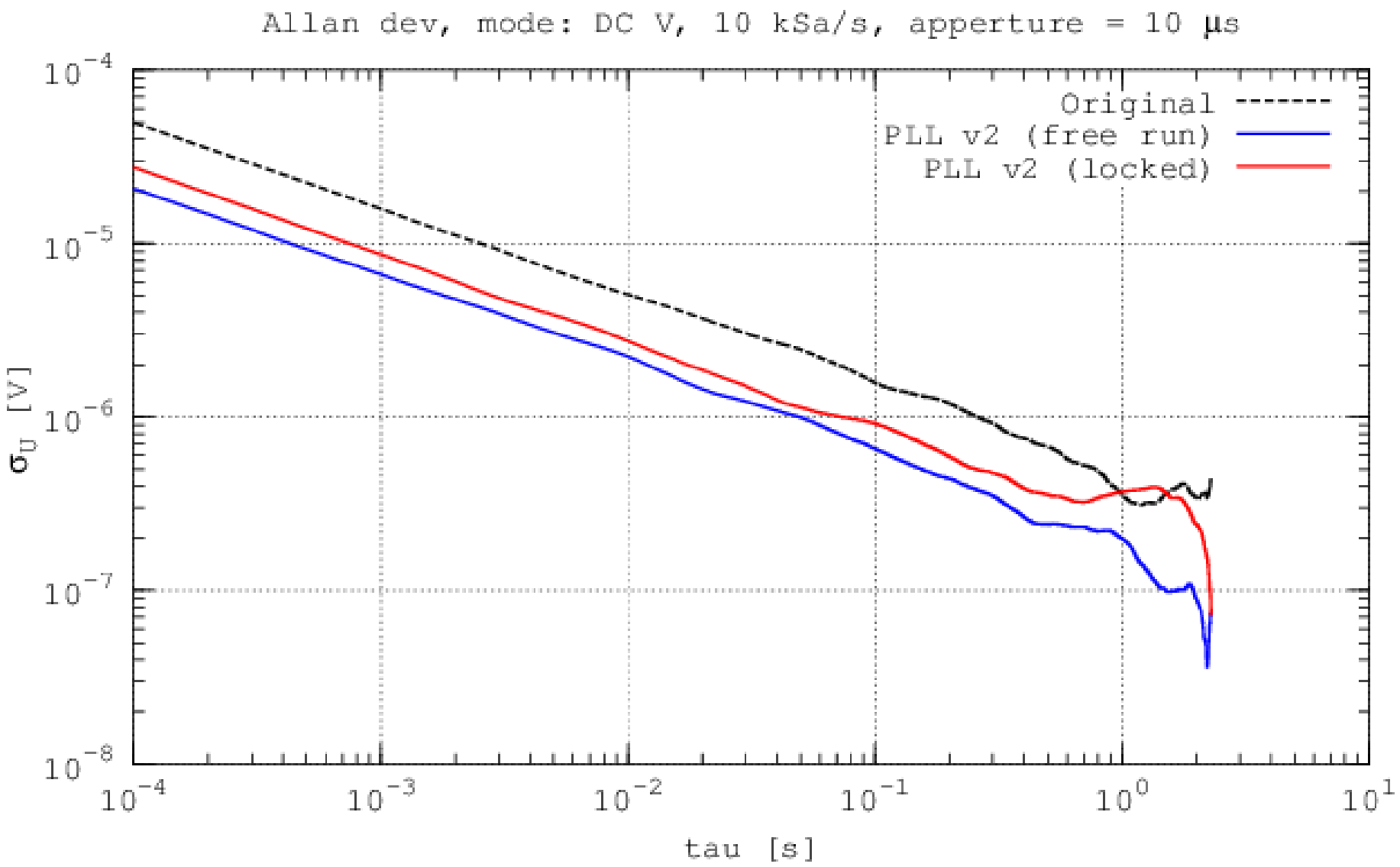


PLL version v2 - testing



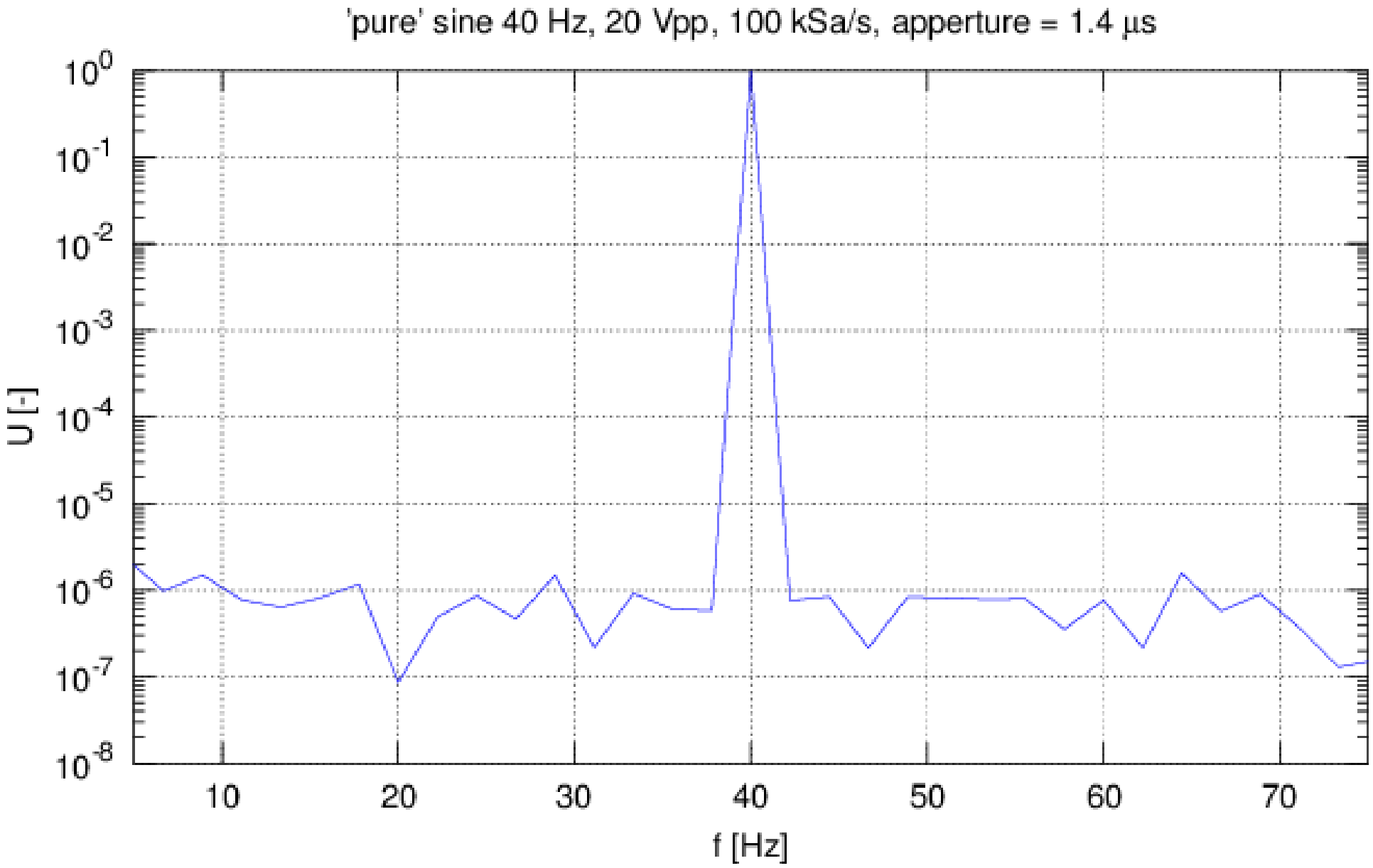
46000 samples, 6 V battery at 10 V range

PLL version v2 - testing

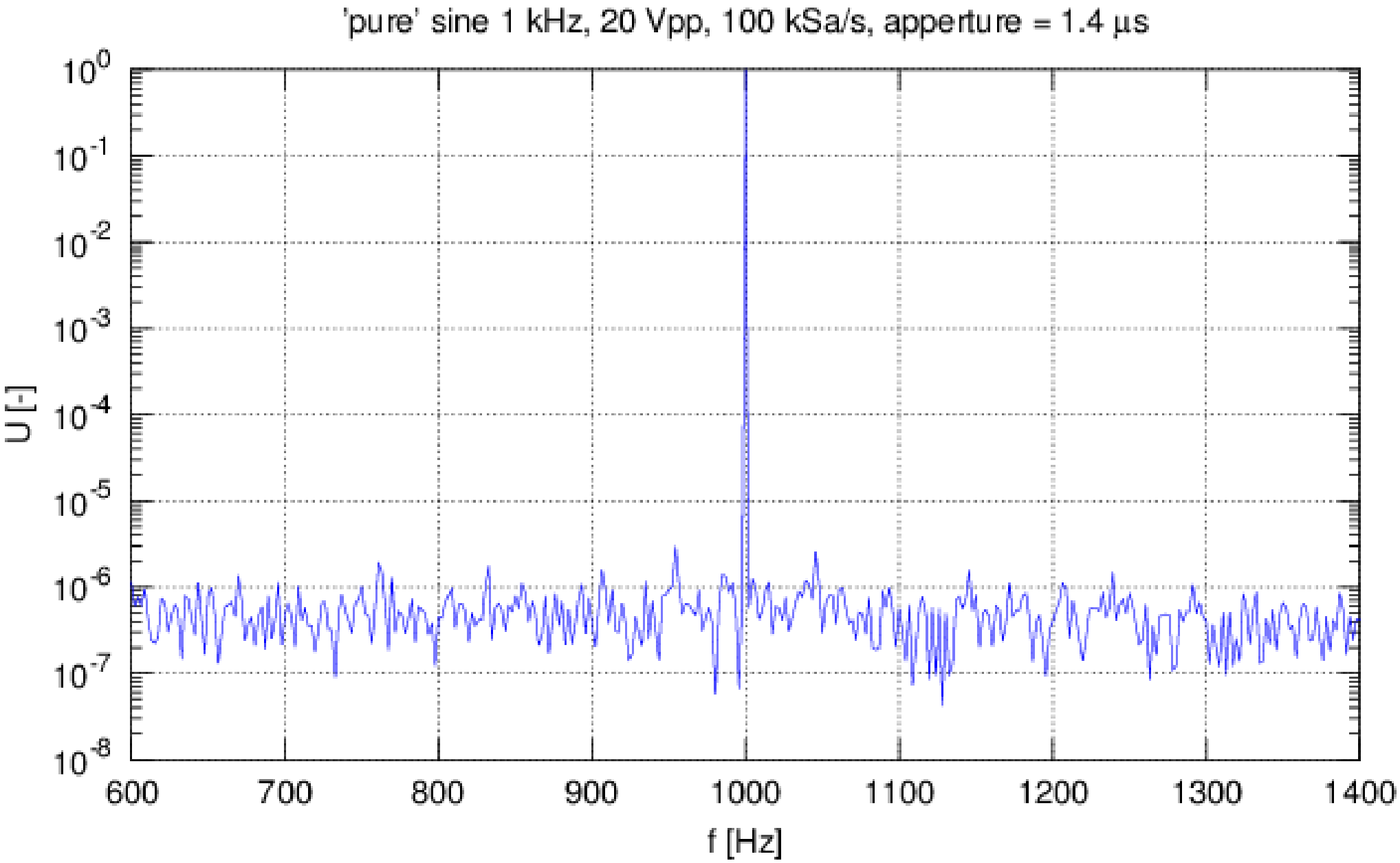


46000 samples, 6 V battery at 10 V range

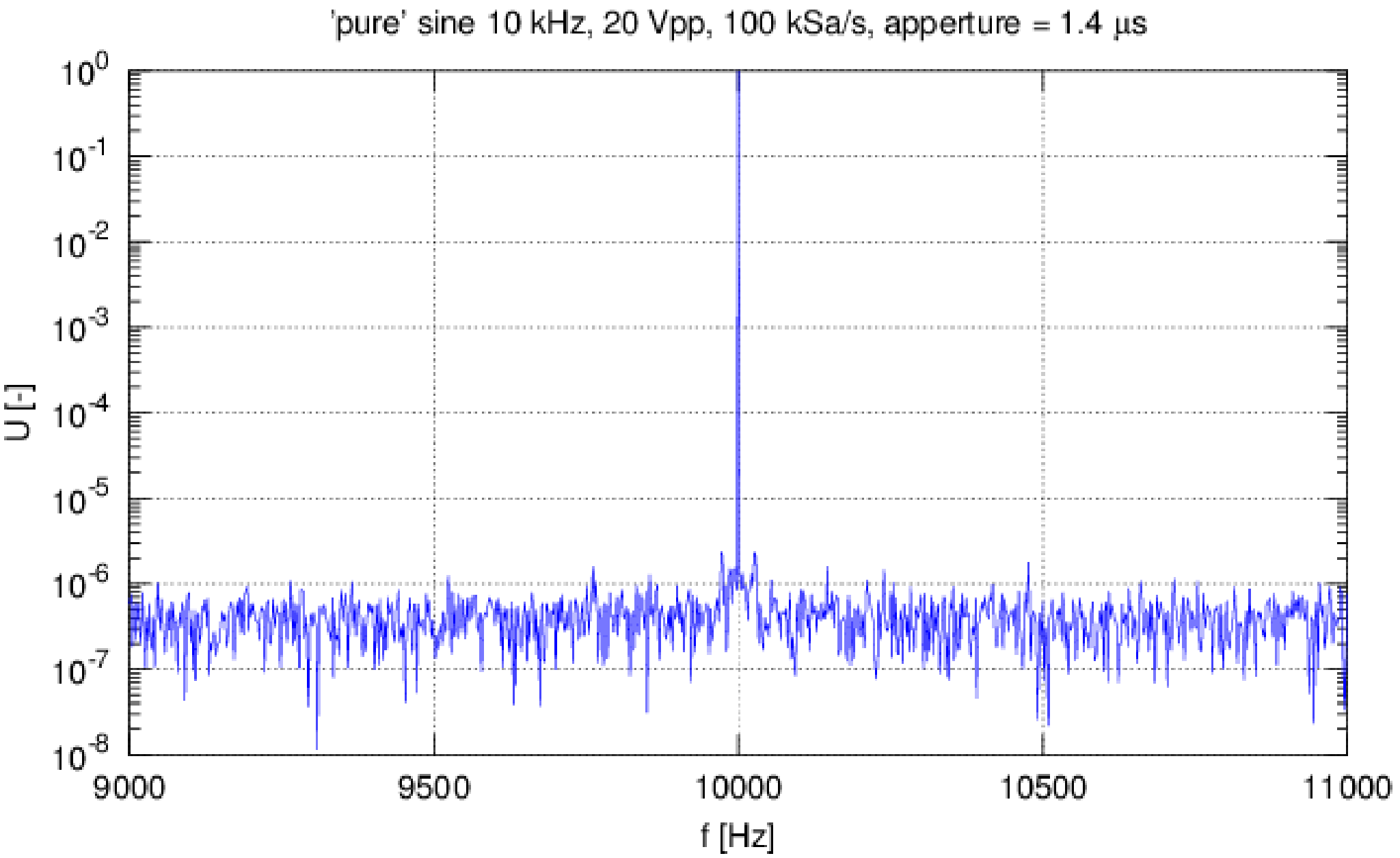
PLL version v2 - testing



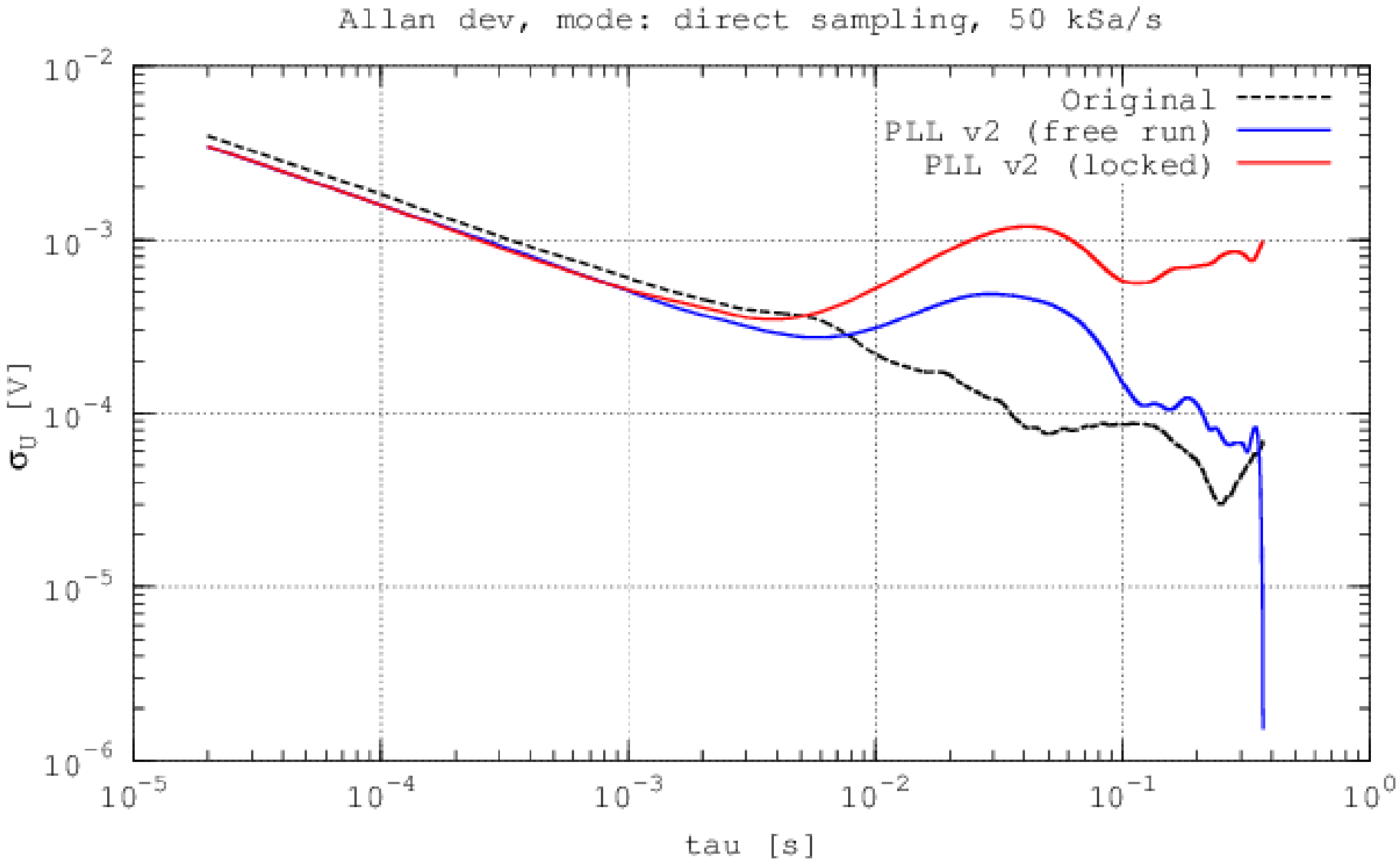
PLL version v2 - testing



PLL version v2 - testing

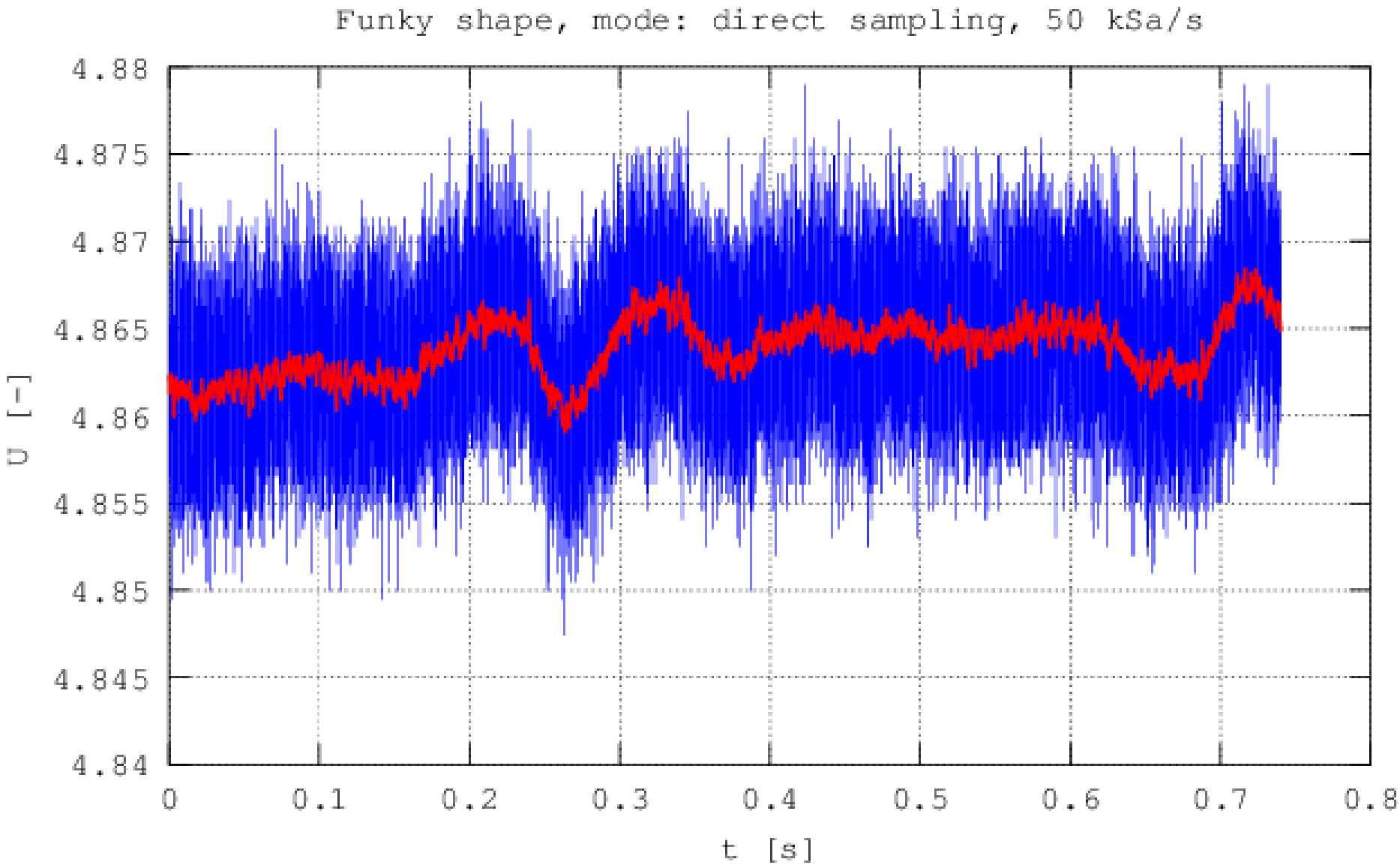


PLL version v2 - testing



37000 samples, 6 V battery at 10 V range

PLL version v2 - testing

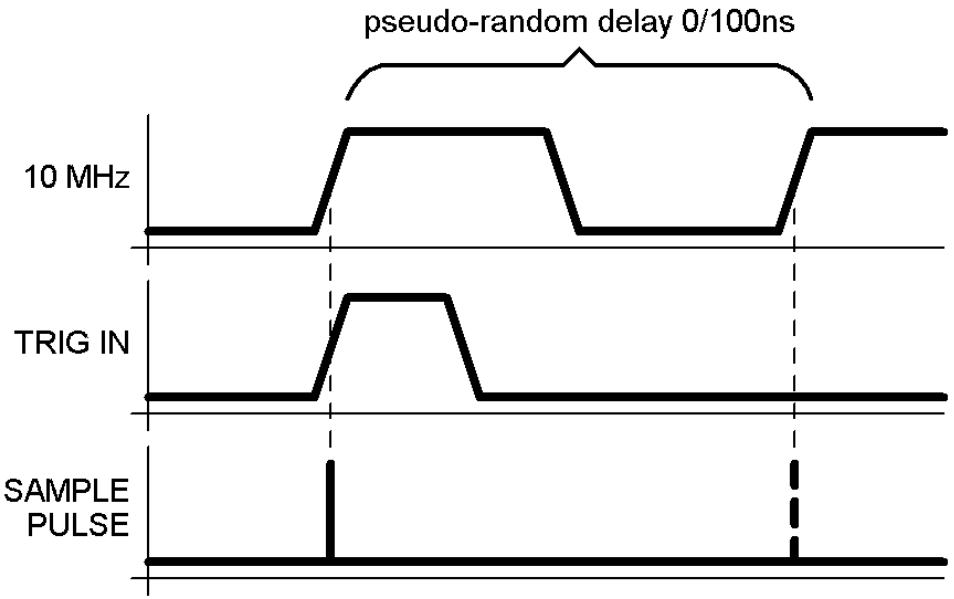


37000 samples, 6 V battery at 10 V range

Conclusion

- Working prototype of PLL module for 3458A

- To do:
  - Select VCTCXO with lower jitter
  - Slower PLL filter
  - Build another piece for second 3458A
  - Solve the triggering problem:



Thank you